High Performance Amorphous Metal-Oxide Semiconductors Thin-Film Passive and Active Pixel Sensors

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Abstract

In this paper, for the first time, we report on high performance amorphous In-Ga-Zn-O (a-IGZO) thin-film transistors (TFTs) based passive pixel sensor (PPS) and active pixel sensor (APS) circuits. Experimental results show that single-TFT PPS with a pitch length of 50μm can achieve a signal charge gain approaching to unity (Gain=0.93) under a fast readout time of 20μs and a dynamic range of 40dB. APS based on three a-IGZO TFTs, with a pitch length of ~100μm, established a high dynamic range of more than 60dB. 2-TFTs half active pixel sensor (H-APS) testing circuits are also designed to investigate the voltage gain ($A_V=\Delta_{VOUT}/\Delta V_G$) properties for the APS circuit in this work. For the a-IGZO APS, A_V is measured to be ~1.25, and through normalization of the pixel capacitance (C_{PIX}) to a common value of 5pF, a large signal charge gain of 25 is obtained.

I. Introduction

Amorphous metal-oxide semiconductors have emerged as potential replacement for amorphous silicon materials in large scale thin-film electronics. Among them, recently amorphous In-Ga-Zn-O thin-film transistors (a-IGZO TFTs) have been intensely investigated in active-matrix display applications [1]. a-IGZO TFTs are also suitable for such applications as photo-sensors, due to their high field-effect mobility (μ_{FE}), low off-current (I_{off}), and low fabrication temperature. In addition, for a-IGZO TFTs, fast transient/readout speed and high signal-to-noise ratio (SNR) compared to conventional amorphous silicon (a-Si:H) technology are expected [2].

II. TFTs and Circuits Fabrication

In this work, all amorphous IGZO TFTs and PPS/APS circuits were fabricated using 4-lithography masks back-channel etching (BCE) process at Lurie Nanofabrication Facility (LNF), University of Michigan. Figure 1 shows the schematic cross section of fabricated TFTs/circuits. The BCE a-IGZO TFTs are fabricated on a glass substrate (TFT-specific glass, AN100 Asahi Glass, Inc.). The glass substrates were firstly cleaned by megasonic. 100-nm-thick molybdenum (Mo) film is then DC sputtered and patterned by dry etching using CF_4 and O_2 gases, as bottom gate electrodes. Next, the PECVD is used for depositing 130-nm-thick silicon oxide (SiO_X) film as field insulator. The 46-nm-thick a-IGZO (1:1:1:4) film is then R. F. sputtered and the active island is defined by wet etching using oxalic acids ($H_2C_2O_4$). Gate-via is performed by using of reactive ion etch (RIE). 260-nm-thick Mo film is then deposited by DC sputtering. Finally, top source/drain electrodes are patterned by back channel etching (BCE) method through wet etching using H_2O_2 etchant.

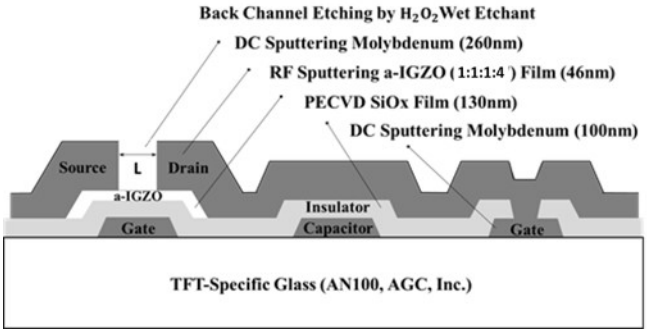

Figure 1. Schematic cross-section of fabricated TFTs and PPS/APS circuits.

III. TFTs Characteristics

The current-voltage (I-V) characteristics of the fabricated a-IGZO TFTs are measured by Agilent B1500A Semiconductor Analyzer. Figure 2 shows the measured I_{DS}-V_{GS} and I_{DS}-V_{DS} characteristics of a-IGZO TFT: W/L=75/4 μm, $I_{OFF}<10^{-12}$A, V_{TH}=6.0V and $\mu_{EFF}=5.62cm^2\cdot V^{-1}\cdot s^{-1}$. The I_{ON}/ I_{OFF} ratio, for V_{DS}= +1V, approaches to ~10^8 and on resistance (R_{ON}) at gate voltage, V_G=+15V, is ~$5\times10^5\Omega$.

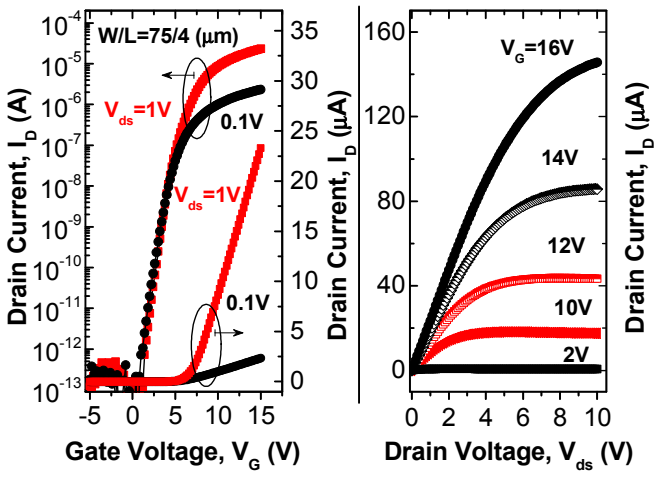

Figure 2. I_{DS}-V_{GS} (left) and I_{DS}-V_{DS} (right) characteristics of a-IGZO TFT: I_{off} < 10^{-12}A, V_{th}=6V, on/off ratio ~10^8 and $\mu_{eff}=5.62cm^2/V\cdot s$. Measured a-IGZO TFT device has a dimension of W/L=75/4 (μm) and gate-to-source overlap length of 4μm.

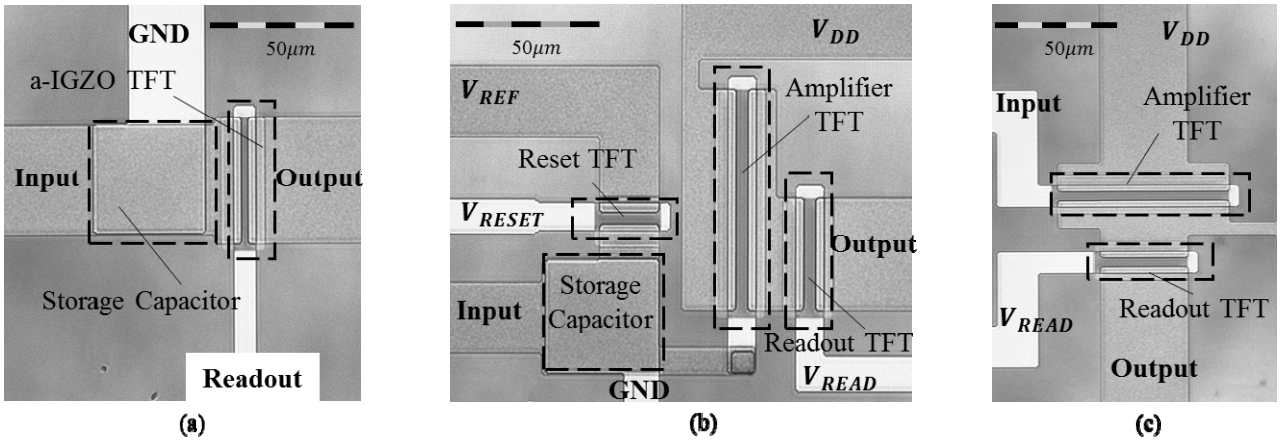

Figure 3. (a) Top view microscopic image of a-IGZO TFT passive pixel sensor (PPS) circuit. The pixel has a compact structure with a pitch length close to 50μm. This small pitch length can allow for high resolution PPS array. (b) Top view microscopic image of a-IGZO active pixel sensor (APS) circuit containing 3 TFTs and a storage capacitor: W_{RESET}=30μm, W_{AMP}=120μm, W_{READ}=60μm, L=10μm and C_{ST}=1pF. The pitch length of pixel is of 135μm. (c) Top view microscopic image of a-IGZO half active pixel sensor (H-APS) circuit, containing 2 TFTs: W_{AMP}=120μm, W_{READ}=60μm, L=10μm. *All circuits are fabricated at Lurie Nanofabrication Facility (LNF) laboratory, University of Michigan, Ann Arbor.

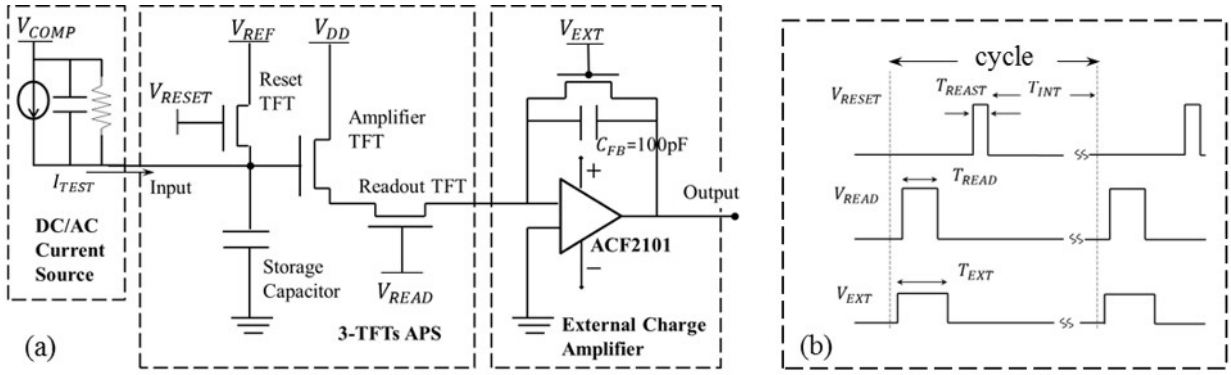

Figure 4. (a) Schematic of 3-TFTs APS circuit with external testing circuit used in electrical characteristics measurements. DC/AC current source provides input testing current (0-10nA) to mimic the light-induced current from photo diodes. Switch-capacitor amplifier (ACF2101) is used to integrate output signal charges, and the feedback capacitance is set to be 100pF. 2 DC voltage sources are connected to provide the constant voltage of V_{REF} and V_{DD}. 3 channels of pulse generators provide the input signals of V_{RESET}, V_{READ} and V_{EXT}. (b) Schematic of the input signal waveforms, including V_{REST}, V_{READ} and V_{EXT}.

IV. Circuits Characteristics

Three kinds of circuits were investigated in this work: a-IGZO PPS, H-APS and APS. As shown in Fig. 3(a), a-IGZO PPS contains a TFT and a storage capacitor. The pixel has a compact structure with a pitch length of ~50μm. This pixel size is suitable for a high resolution PPS arrays. This small pitch length can allow for high resolution PPS array. Figure 3 (b) and (c) illustrated the top view microscopic images of a-IGZO APS and H-APS pixel circuits. a-IGZO APS contains 3 TFTs, two of which are used as switching elements for reset and readout respectively and another one is used as an inner amplifier, as well as a connected storage capacitance. The pixel has a compact structure with a pitch length of only 135μm, which is much smaller when compared to a-Si:H 3-TFTs APS [3]. For H-APS circuit, two a-IGZO TFTs are series connected: one is to mimic the amplifier TFT and the other one is for readout switch TFT. The H-APS circuit is designed to analyze the voltage gain of APS circuit in this work.

To characterize the electrical properties of these circuits, different measured systems were set up. The PPS circuit are characterized by the measurement system, which is proposed by G. Yoo et al. [4] for hemispheric a-Si:H PPS. V_{READ} is set to be +18V/-2V, readout time (T_{READ}) is set to be 20μs and input current time (T_{INT}) is 16ms. To measure the APS circuit electrical properties, a developed measurement system is proposed. Figure 4 (a) shows the schematic diagram of 3-TFTs APS circuit with external testing circuits used in electrical measurement system. DC/AC current source generates input testing current (0-10nA) to mimic the light-induced currents from photo diodes. Switch-capacitor amplifier ACF2101 is used to integrate output signal charges and three pulse generators are used to provide operational driving signals. Schematic of these driving waveforms are shown in Fig. 4(b). To characterize H-APS, Agilent B1500A is used to acquire I-V properties. The same external charge amplifier circuit shown in Figure 4 (a) is used in acquiring output voltage (V_{OUT}) vs. input voltage bias (V_{BIAS}) plots.

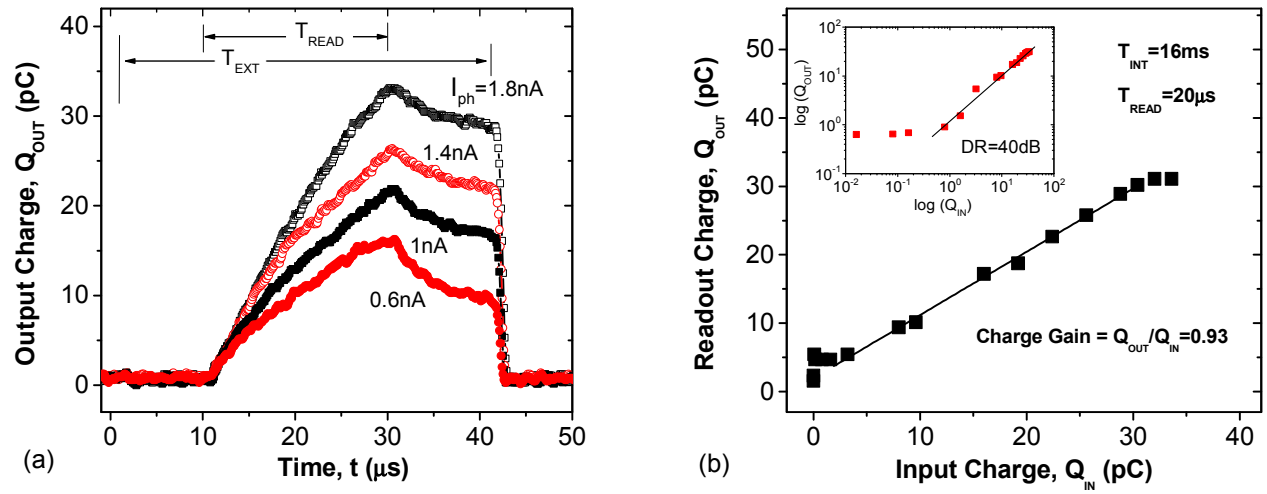

Figure 5. (a) Oscilloscope traced output signal charge for different input testing current (0-1.8nA) of the a-IGZO TFT PPS. (b) Linear plot of oscilloscope traced output signal charge sampling at 38µs vs. input charges. The signal charge gain extracted from the data is ~0.93 in linear working regime. Logarithmic scale plot, shown in inset, illustrates the PPS operation dynamic range (DR) of ~40dB.

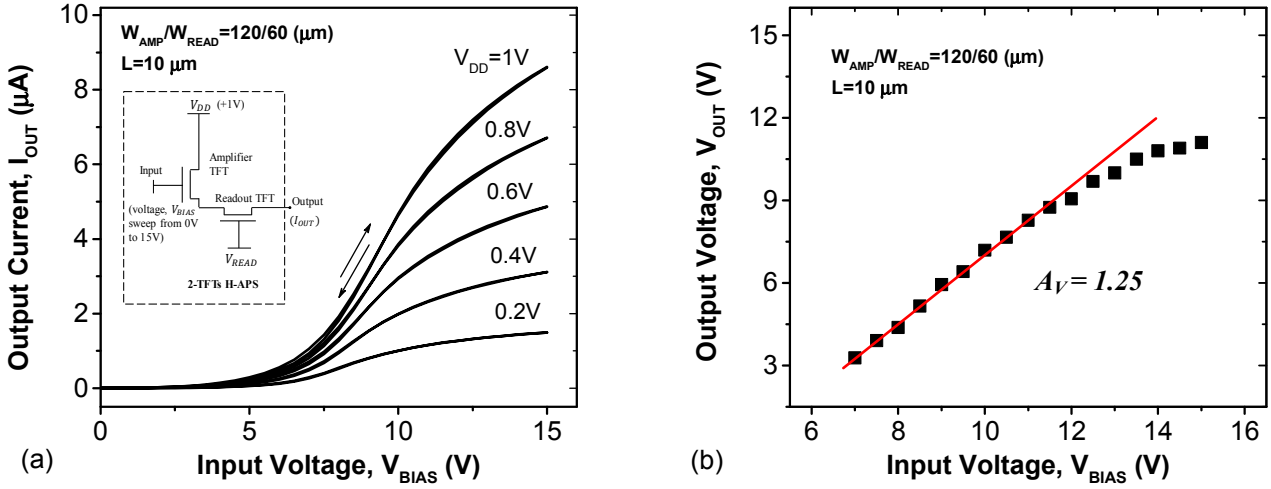

Figure 6. (a) Current-voltage (I-V) characteristics of 2-TFTs H-APS testing circuits where W_{AMP}/W_{READ}=120/60 µm, L=10µm. V_{READ} is set to be +18V. V_{DD} sweeps from 0 to 1V. (b) Plots of output voltage read on feedback capacitor vs. input voltages for 2-TFTs H-APS, showing a voltage gain of 1.25 for the input bias voltages from 7 to 12V.

IV.i. a-IGZO TFT PPS Electrical Properties

Figure 5 (a) shows the signal charge integrated on the external charge amplifier feedback capacitor (C_{FB}) traced by oscilloscope for different input testing current. In each cycle, input charges are initially stored on the storage capacitor during the integration period, following:

$$Q_{INPUT} = I_{ph} \times T_{INT} \qquad (1)$$

Then these charges start to move to C_{FB} during the readout period, when the a-IGZO TFT turns on, for 20µs (T_{READ}). From the figure, we can observe that within only 20µs, more than 93 percent of charge has been transferred to the feedback capacitor from storage capacitor. It indicates the a-IGZO PPS has a much faster readout speed than conventional a-Si:H TFTs PPS [3, 4]. Figure 5 (b) shows the linear plots of output signal charge sampled at 38µs vs. input charge. From the plots, we can see that when in its linearly working regime, the a-IGZO PPS shows a signal charge gain is of ~0.93 and the inset logarithmic scale plots illustrates dynamic range (DR) is of 40dB.

$$Charge\ Gain = \Delta Q_{OUT}/\Delta Q_{INPUT} \qquad (2)$$

$$DR = 20 \times \log(Q_{SIGNAL,MAX}/Q_{SIGNAL,MIN}) \qquad (3)$$

IV.ii. a-IGZO TFTs H-APS Electrical Properties

Current-voltage (I-V) curves for H-APS is shown in Fig. 6(a), where V_{READ} is set to be +18V. Input bias voltage sweeps from 0 to +15V and +15 to 0V, where

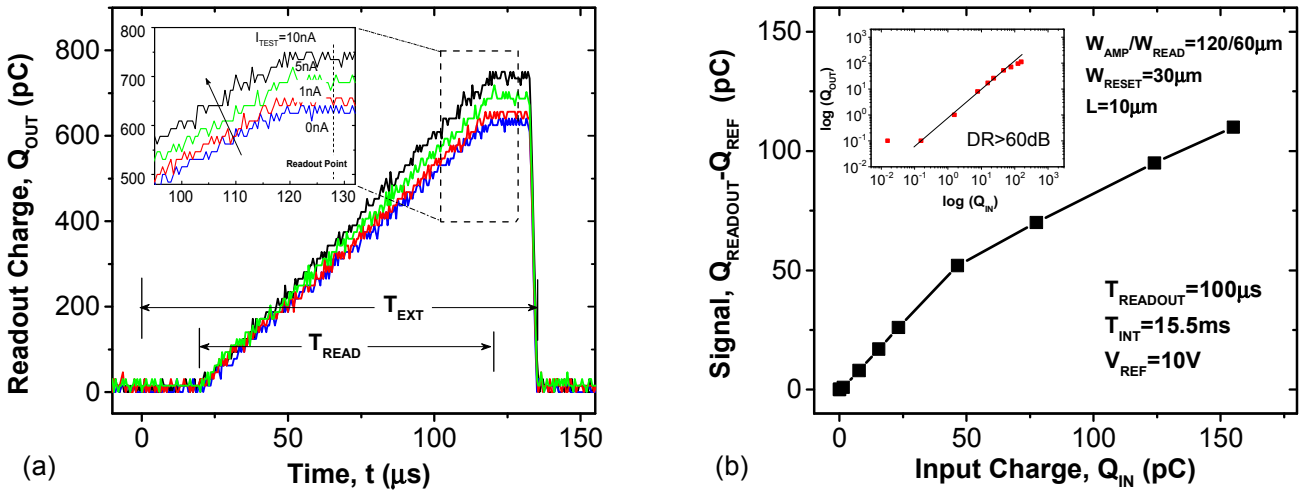

Figure 7. (a) Oscilloscope traced output signal charge for different input testing current (0-10nA) of the a-IGZO 3-TFTs APS: W/L for reset, amplifier and readout TFTs are 30/10, 120/10 and 60/10 (µm), respectively. The V_{REF}, V_{RESET}, V_{READ} and V_{DD} are set to be +10V, -2V/+18V, -2V/+18Vand +1V. T_{INT} and $T_{READOUT}$ are 15.5ms and 100µs. (b) Plots of output signal charge vs. input charge, V_{REF} is set to be 10V. Logarithmic scale plots, shown in inset, illustrates the APS operation dynamic range (DR) of more than 60dB.

negligible hysteresis is observed. It shows very good stability. The parameters extracted from these I-V curves can be helpful in optimizing the driving signals for APS. Figure 6 (b) illustrates the linear plots of output voltage read out on feedback capacitor vs. input voltage bias for the H-APS. From the plots, in a specific region, we can observe a linear relationship with a slope of 1.25, which is, in fact, the value of voltage gain (A_V):

$$A_V = V_{OUT}/V_{IN} \qquad (4)$$

Recalling:

$$Charge\ Gain = A_V \times (C_{FB}/C_{PIX}) \qquad (5)$$

we could obtain the Gain as large as 25, when we normalize the C_{PIX} to a common value of 5pF [3].

IV.iii. a-IGZO TFTs APS Electrical Properties

Figure 7 (a) shows the signal charge integrated on the C_{FB} traced by oscilloscope for different input testing current for a-IGZO APS. Reference voltage (V_{REF}) and V_{DD} are set as +10V and +1V and readout time is set to be 100µs. The low value of V_{DD} (+1V) indicates the a-IGZO APS will require low power consumption. Linear plot of output signal charge vs. input charge is shown in Fig. 7 (b) and inset logarithmic scale plot illustrates dynamic range for the a-IGZO APS of 61dB. These attractive properties are very interesting to those applications requiring high sensitivity.

V. Important of This Work

In this work, we firstly report and demonstrated the PPS/APS concepts by using of the same amorphous semiconductor techniques and fabrication process methods as those used in modern displays. Thanks to the higher mobility, low off-current properties of a-IGZO TFTs, when compared to a-Si:H, for the first time, we acquire the possibility to realize the integration of both modern display and imager/detectors on the same substrate (glass). This new ability can allow us not only dramatically reduces the dimension of those terminal equipment which requires both display and imager/detectors, such as night vision equipment and future wearable smart devices, but also simplify the module structure. Finally, the developed technology can be used for generation of the X-ray detectors.

VI. Possible Applications

The a-IGZO PPS/APS techniques reported in this work could lend to development of future high performance medical X-ray detector for tomosynthesis, Full-of-View (FOV) digital camera and IR night vision detectors and fully integrated displays.

VII. Conclusion

PPS and APS circuits based on a-IGZO TFTs were successfully designed, fabricated and characterized in this work. For the first time, the electrical properties of both a-IGZO PPS and APS have been reported. The small pitch length and fast readout speed properties of PPS, and high dynamic range as well as large signal gain properties of APS all indicate that a-IGZO TFTs based PPS/APS are very promising in future imaging and display applications.

References

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